



4/8 Channel Fault-Protected Analog Multiplexers

ADG508F/ADG509F/ADG528F*

FEATURES

- Low On Resistance (300 Ω typ)
- Fast Switching Times
 - t_{ON} 250 ns max
 - t_{OFF} 250 ns max
- Low Power Dissipation (3.3 mW max)
- Fault and Overvoltage Protection
- All Switches OFF with Power Supply OFF
- Analog Output of ON Channel Clamped Within Power Supplies If an Overvoltage Occurs
- Latch-Up Proof Construction
- Break Before Make Construction
- TTL and CMOS Compatible Inputs

APPLICATIONS

- Existing Multiplexer Applications (Both Fault-Protected and Non-Fault-Protected)
- New Designs Requiring Multiplexer Functions

GENERAL DESCRIPTION

The ADG508F, ADG509F and ADG528F are CMOS analog multiplexers, the ADG508F and ADG528F comprising 8 single channels and the ADG509F comprising four differential channels. These multiplexers provide fault protection. Using a series n-channel, p-channel, n-channel MOSFET structure, both device and signal source protection is provided in the event of an overvoltage or power loss. The multiplexer can withstand continuous overvoltage inputs up to ± 35 V. During fault conditions, the multiplexer input (or output) appears as an open circuit and only a few nanoamperes of leakage current will flow. This protects not only the multiplexer and the circuitry driven by the multiplexer, but also protects the sensors or signal sources which drive the multiplexer.

The ADG508F and ADG528F switch one of eight inputs to a common output as determined by the 3-bit binary address lines A0, A1 and A2. The ADG509F switches one of four differential inputs to a common differential output as determined by the 2-bit binary address lines A0 and A1. The ADG528F has on-chip address and control latches that facilitate microprocessor interfacing. An EN input on each device is used to enable or disable the device. When disabled, all channels are switched OFF.

PRODUCT HIGHLIGHTS

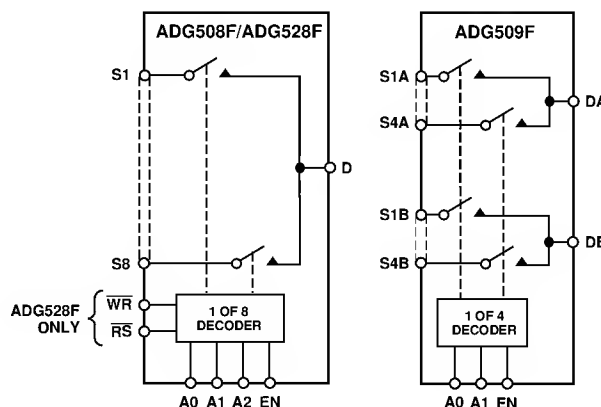
- Fault Protection.
The ADG508F/ADG509F/ADG528F can withstand continuous voltage inputs up to ± 35 V. When a fault occurs due to the power supplies being turned off, all the channels

*Patent pending.

REV. A

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FUNCTIONAL BLOCK DIAGRAMS



are turned off and only a leakage current of a few nanoamperes flows.

- ON channel turns off while fault exists.
- Low R_{ON} .
- Fast Switching Times.
- Break-Before-Make Switching.
Switches are guaranteed break-before-make so that input signals are protected against momentary shorting.
- Trench Isolation Eliminates Latch-up.
A dielectric trench separates the p and n-channel MOSFETs thereby preventing latch-up.

ORDERING GUIDE

Model ¹	Temperature Range	Package Option ²
ADG508FBN	-40°C to +85°C	N-16
ADG508FB RN	-40°C to +85°C	R-16N
ADG508FBRW	-40°C to +85°C	R-16W
ADG508FTQ	-55°C to +125°C	Q-16
ADG509FBN	-40°C to +85°C	N-16
ADG509FB RN	-40°C to +85°C	R-16N
ADG509FBRW	-40°C to +85°C	R-16W
ADG509FTQ	-55°C to +125°C	Q-16
ADG528FBN	-40°C to +85°C	N-18
ADG528FBP	-40°C to +85°C	P-20A
ADG528FTQ	-55°C to +125°C	Q-18

NOTES

¹To order MIL-STD-883, Class B processed parts, add /883B to T grade part numbers.

²N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip;
RN = 0.15" Small Outline IC (SOIC), RW = 0.3" Small Outline IC (SOIC).

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703

ADG508F/ADG509F/ADG528F—SPECIFICATIONS¹

Dual Supply ($V_{DD} = +15\text{ V} \pm 10\%$, $V_{SS} = -15\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted)

	B Version −40°C to		T Version −55°C to			
Parameter	+25°C	+85°C	+25°C	+125°C	Units	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range		$V_{SS} + 3$ $V_{DD} - 1.5$		$V_{SS} + 3$ $V_{DD} - 1.5$	V min V max	$-10\text{ V} \leq V_S \leq +10\text{ V}$, $I_S = 1\text{ mA}$; $V_{DD} = +15\text{ V} \pm 10\%$, $V_{SS} = -15\text{ V} \pm 10\%$ $-10\text{ V} \leq V_S \leq +10\text{ V}$, $I_S = 1\text{ mA}$; $V_{DD} = +15\text{ V} \pm 5\%$, $V_{SS} = -15\text{ V} \pm 5\%$ $V_S = 0\text{ V}$, $I_S = 1\text{ mA}$ $V_S = 0\text{ V}$, $I_S = 1\text{ mA}$
R_{ON}	300	350	300	400	Ω typ	
		400		450	Ω max	
R_{ON} Drift	0.6		0.6		%/°C typ	
R_{ON} Match	5		5		% max	
LEAKAGE CURRENTS						
Source OFF Leakage I_S (OFF)	± 0.02 ± 1	± 50	± 0.02 ± 1	± 50	nA typ nA max	$V_D = \pm 10\text{ V}$, $V_S = \mp 10\text{ V}$; Test Circuit 2
Drain OFF Leakage I_D (OFF)	± 0.04		± 0.04		nA typ	$V_D = \pm 10\text{ V}$, $V_S = \mp 10\text{ V}$; Test Circuit 3
ADG508F/ADG528F	± 1	± 60	± 1	± 200	nA max	
ADG509F	± 1	± 30	± 1	± 100	nA max	
Channel ON Leakage I_D , I_S (ON)	± 0.04		± 0.04		nA typ	$V_S = V_D = \pm 10\text{ V}$; Test Circuit 4
ADG508F/ADG528F	± 1	± 60	± 1	± 200	nA max	
ADG509F	± 1	± 30	± 1	± 100	nA max	
FAULT						
Output Leakage Current (With Overvoltage)	± 0.02 ± 2	± 2	± 0.02 ± 2		nA typ μA max	$V_S = \pm 33\text{ V}$, $V_D = 0\text{ V}$, Test Circuit 3
Input Leakage Current (With Overvoltage)	± 0.005 ± 2		± 0.005 ± 2		μA typ μA max	$V_S = \pm 25\text{ V}$, $V_D = \mp 10\text{ V}$, Test Circuit 5
Input Leakage Current (With Power Supplies OFF)	± 0.001 ± 2		± 0.001 ± 2		μA typ μA max	$V_S = \pm 25\text{ V}$, $V_D = V_{EN} = A0, A1, A2 = 0\text{ V}$ Test Circuit 6
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	$V_{IN} = 0\text{ or }V_{DD}$
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current I_{INL} or I_{INH}		± 1		± 1	μA max	
C_{IN} , Digital Input Capacitance	5		5		pF typ	
DYNAMIC CHARACTERISTICS ²						
$t_{TRANSITION}$	200 300	400	200 300	400	ns typ ns max	$R_L = 1\text{ M}\Omega$, $C_L = 35\text{ pF}$; $V_{S1} = \pm 10\text{ V}$, $V_{S8} = \mp 10\text{ V}$; Test Circuit 7
t_{OPEN}	50		50		ns typ	$R_L = 1\text{ k}\Omega$, $C_L = 35\text{ pF}$; $V_S = +5\text{ V}$; Test Circuit 8
t_{ON} (EN, \overline{WR})	25 200	10	25 200	10	ns min ns typ	$R_L = 1\text{ k}\Omega$, $C_L = 35\text{ pF}$; $V_S = +5\text{ V}$; Test Circuit 9
t_{OFF} (EN, \overline{RS})	250 200	400	250 200	400	ns max ns typ	$R_L = 1\text{ k}\Omega$, $C_L = 35\text{ pF}$; $V_S = +5\text{ V}$; Test Circuit 9
t_{SETT} , Settling Time					ns max	
0.1%		1		1	μs typ	$R_L = 1\text{ k}\Omega$, $C_L = 35\text{ pF}$; $V_S = +5\text{ V}$
0.01%		2.5		2.5	μs typ	
ADG528F Only						
t_W , Write Pulse Width	100	120	100	200	ns min	$V_S = 0\text{ V}$, $R_S = 0\text{ }\Omega$, $C_L = 1\text{ nF}$; Test Circuit 12 $R_L = 1\text{ k}\Omega$, $C_L = 15\text{ pF}$, $f = 100\text{ kHz}$; $V_S = 7\text{ V rms}$; Test Circuit 13
t_S , Address, Enable Setup Time		100		100	ns min	
t_H , Address, Enable Hold Time		10		10	ns min	
t_{RS} , Reset Pulse Width		100		100	ns min	
Charge Injection	4		4		pC typ	
OFF Isolation	68 50		68 50		dB typ dB min	
C_S (OFF)	5		5		pF typ	
C_D (OFF)						
ADG508F/ADG528F	50		50		pF typ	
ADG509F	25		25		pF typ	
POWER REQUIREMENTS						
I_{DD}	0.05 0.2	0.5	0.05 0.2	0.5	mA typ mA max	$V_{IN} = V_{INL}$ or V_{INH}
I_{SS}	0.01 0.1	0.1	0.01 0.1	0.2	mA typ mA max	
I_{DD}	0.1	0.2	0.1	0.2	mA max	$V_{IN} = 0\text{ V}$ or 5 V
I_{SS}	0.1	0.1	0.1	0.1	mA max	

NOTES

¹Temperature ranges are as follows: B Version: −40°C to +85°C; T Version: −55°C to +125°C.

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ADG508F/ADG509F/ADG528F

Table I. ADG508F Truth Table

A2	A1	A0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

X = Don't Care

Table II. ADG509F Truth Table

A1	A0	EN	ON SWITCH PAIR
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

X = Don't Care

Table III. ADG528F Truth Table

A2	A1	A0	EN	\overline{WR}	\overline{RS}	ON SWITCH
X	X	X	X	\uparrow	1	Retains Previous Switch Condition
X	X	X	X	X	0	NONE (Address and Enable Latches Cleared)
X	X	X	0	0	1	NONE
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

X = Don't Care

TIMING DIAGRAMS (ADG528F)

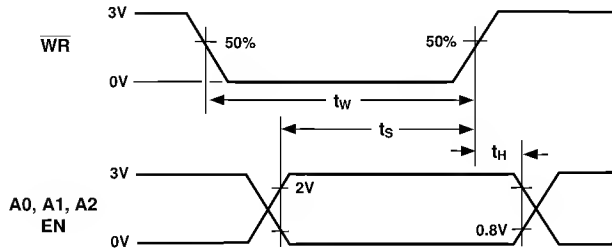


Figure 1.

Figure 1 shows the timing sequence for latching the switch address and enable inputs. The latches are level sensitive; therefore, while \overline{WR} is held low, the latches are transparent and the switches respond to the address and enable inputs. This input data is latched on the rising edge of \overline{WR} .

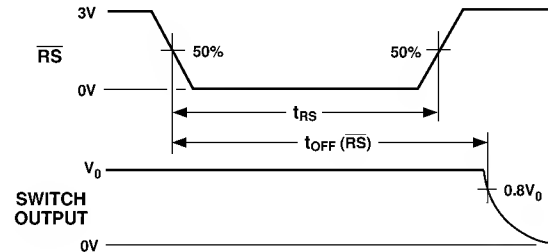


Figure 2.

Figure 2 shows the Reset Pulse Width, t_{RS} , and the Reset Turn off Time, $t_{OFF}(\overline{RS})$.

Note: All digital input signals rise and fall times are measured from 10% to 90% of 3 V. $t_R = t_F = 20$ ns.

ADG508F/ADG509F/ADG528F

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to V_{SS} +44 V
V_{DD} to GND -0.3 V to +25 V
V_{SS} to GND +0.3 V to -25 V
V_{EN}, V_A Digital Input -0.3 V to V_{DD} + 2 V or 20 mA,
Which ever Occurs First
V_S, Analog Input Overvoltage with Power ON V_{SS} - 20 V
to V_{DD} + 20 V

V_S, Analog Input Overvoltage with Power OFF
..... -35 V to +35 V
Continuous Current, S or D 20 mA
Peak Current, S or D
(Pulsed at 1 ms, 10% Duty Cycle max) 40 mA

Operating Temperature Range

Industrial (B Version) -40°C to +85°C
Extended (T Version) -55°C to +125°C
Storage Temperature Range -65°C to +150°C
Junction Temperature +150°C

Cerdip Package

θ_{JA}, Thermal Impedance

16-Pin 76°C/W

18-Pin 73°C/W

Lead Temperature, Soldering (10 sec) +300°C

Plastic Package

θ_{JA}, Thermal Impedance

16-Pin 117°C

18-Pin 110°C

Lead Temperature, Soldering (10 sec) +260°C

SOIC Package

θ_{JA}, Thermal Impedance

Narrow Body 77°C/W

Wide Body 75°C/W

Lead Temperature, Soldering

Vapor Phase (60 sec) +215°C

Infrared (15 sec) +220°C

PLCC Package

θ_{JA}, Thermal Impedance 90°C/W

Lead Temperature, Soldering

Vapor Phase (60 sec) +215°C

Infrared (15 sec) +220°C

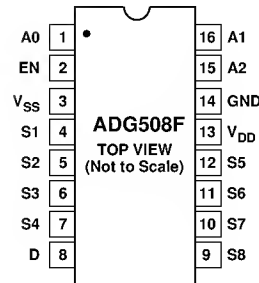
*Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

CAUTION

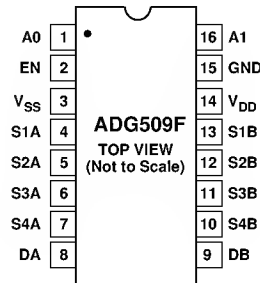
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although these devices feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ADG508F/ADG509F PIN CONFIGURATIONS

DIP/SOIC

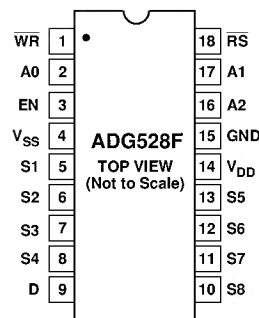


DIP/SOIC

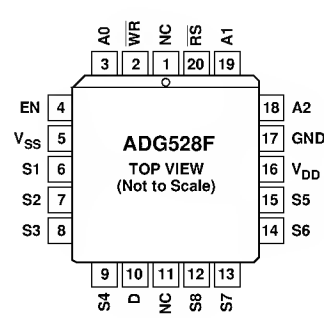


ADG528F PIN CONFIGURATIONS

DIP



PLCC



TERMINOLOGY

V_{DD}	Most positive power supply potential.
V_{SS}	Most negative power supply potential.
GND	Ground (0 V) reference.
R_{ON}	Ohmic resistance between D and S.
R_{ON} Drift	Change in R_{ON} when temperature changes by one degree Celsius.
R_{ON} Match	Difference between the R_{ON} of any two channels.
I_S (OFF)	Source leakage current when the switch is off.
I_D (OFF)	Drain leakage current when the switch is off.
I_D, I_S (ON)	Channel leakage current when the switch is on.
V_D (V_S)	Analog voltage on terminals D, S.
C_S (OFF)	Channel input capacitance for “OFF” condition.
C_D (OFF)	Channel output capacitance for “OFF” condition.
C_D, C_S (ON)	“ON” switch capacitance.
C_{IN}	Digital input capacitance.
t_{ON} (EN)	Delay time between the 50% and 90% points of the digital input and switch “ON” condition.
t_{OFF} (EN)	Delay time between the 50% and 90% points of the digital input and switch “OFF” condition.
$t_{TRANSITION}$	Delay time between the 50% and 90% points of the digital inputs and the switch “ON” condition when switching from one address state to another.
t_{OPEN}	“OFF” time measured between 80% points of both switches when switching from one address state to another.
V_{INL}	Maximum input voltage for Logic “0”.
V_{INH}	Minimum input voltage for Logic “1”.
I_{INL} (I_{INH})	Input current of the digital input.
Off Isolation	A measure of unwanted signal coupling through an “OFF” channel.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
I_{DD}	Positive supply current.
I_{SS}	Negative supply current.

Typical Performance Graphs

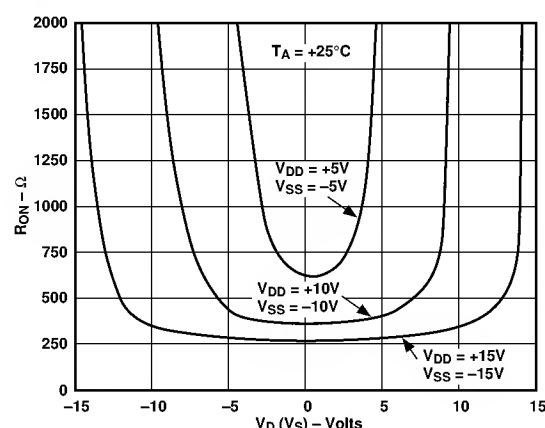


Figure 3. On Resistance as a Function of V_D (V_S)

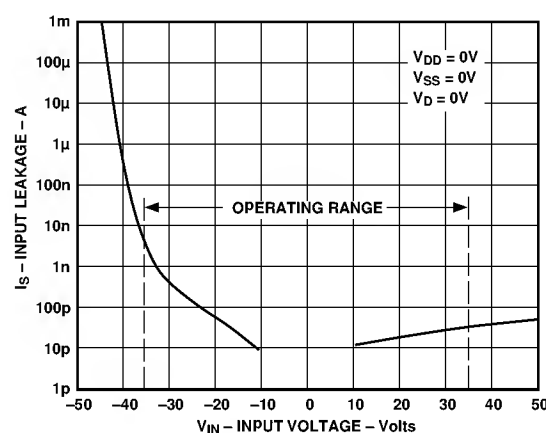


Figure 4. Input Leakage Current as a Function of V_S (Power Supplies OFF) During Overvoltage Conditions

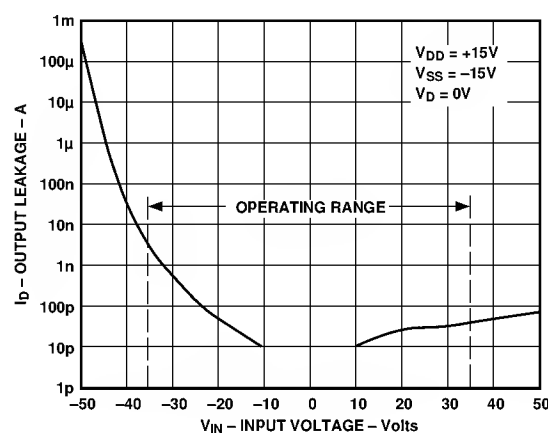


Figure 5. Output Leakage Current as a Function of V_S (Power Supplies ON) During Overvoltage Conditions

ADG508F/ADG509F/ADG528F

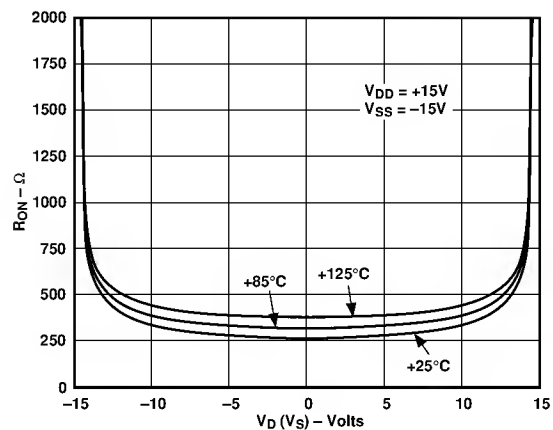


Figure 6. On Resistance as a Function of V_D (V_S) for Different Temperatures

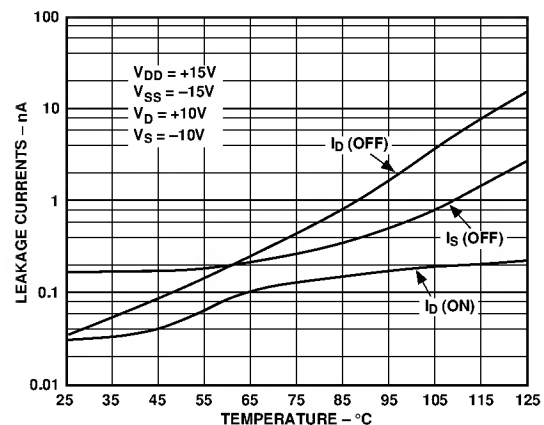


Figure 9. Leakage Currents as a Function of Temperature

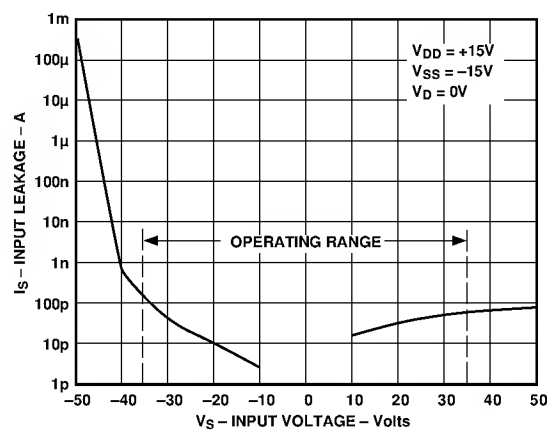


Figure 7. Input Leakage Current as a Function of V_S (Power Supplies ON) During Overvoltage Conditions

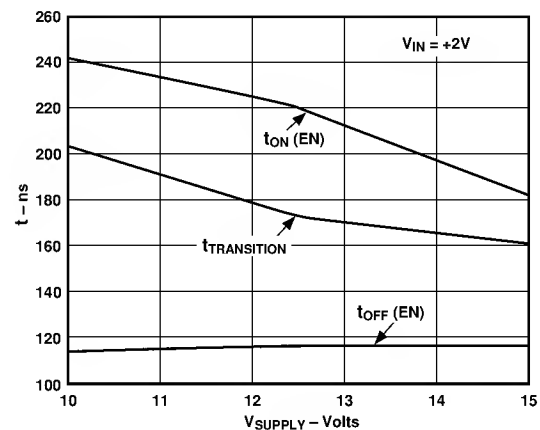


Figure 10. Switching Time vs. Power Supply

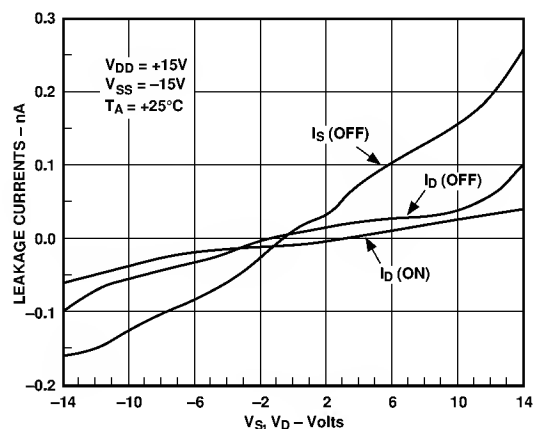


Figure 8. Leakage Currents as a Function of V_D (V_S)

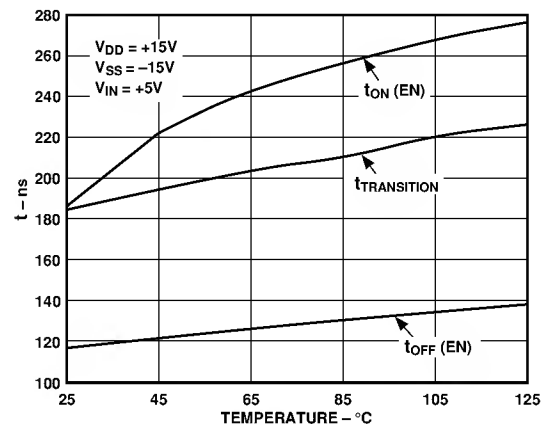


Figure 11. Switching Time vs. Temperature

THEORY OF OPERATION

The ADG508F/ADG509F/ADG528F multiplexers are capable of withstanding overvoltages up to ± 35 V, irrespective of whether the power supplies are present or not. Each channel of the multiplexer consists of an n-channel MOSFET, a p-channel MOSFET and an n-channel MOSFET, connected in series. When the analog input exceeds the power supplies, one of the MOSFETs will switch off, limiting the current to sub-microamp levels, thereby preventing the overvoltage from damaging any circuitry following the multiplexer. Figure 12 illustrates the channel architecture that enables these multiplexers to withstand continuous overvoltages.

When an analog input of $V_{SS} + 3$ V to $V_{DD} - 1.5$ V is applied to the ADG508F/ADG509F/ADG528F, the multiplexer behaves as a standard multiplexer, with specifications similar to a standard multiplexer, for example, the on-resistance is 400 Ω maximum. However, when an overvoltage is applied to the device, one of the three MOSFETs will turn off.

Figures 12 to 15 show the conditions of the three MOSFETs for the various overvoltage situations. When the analog input applied to an ON channel approaches the positive power supply line, the n-channel MOSFET turns OFF since the voltage on the analog input exceeds the difference between V_{DD} and the

n-channel threshold voltage (V_{TN}). When a voltage more negative than V_{SS} is applied to the multiplexer, the p-channel MOSFET will turn off since the analog input is more negative than the difference between V_{SS} and the p-channel threshold voltage (V_{TP}). Since V_{TN} is nominally 1.5 V and V_{TP} is typically 3 V, the analog input range to the multiplexer is limited to -12 V to $+13.5$ V when a ± 15 V power supply is used.

When the power supplies are present but the channel is off, again either the p-channel MOSFET or one of the n-channel MOSFETs will turn off when an overvoltage occurs.

Finally, when the power supplies are off, the gate of each MOSFET will be at ground. A negative overvoltage switches on the first n-channel MOSFET but the bias produced by the overvoltage causes the p-channel MOSFET to remain turned off. With a positive overvoltage, the first MOSFET in the series will remain off since the gate to source voltage applied to this MOSFET is negative.

During fault conditions, the leakage current into and out of the ADG508F/ADG509F/ADG528F is limited to a few microamps. This protects the multiplexer and succeeding circuitry from over stresses as well as protecting the signal sources which drive the multiplexer. Also, the other channels of the multiplexer will be undisturbed by the overvoltage and will continue to operate normally.

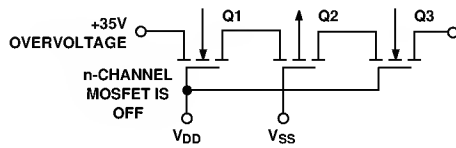


Figure 12. +35 V Overvoltage Input to the ON Channel

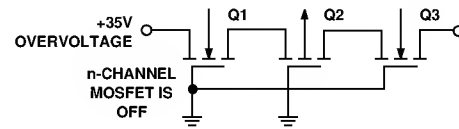


Figure 14. +35 V Overvoltage with Power OFF

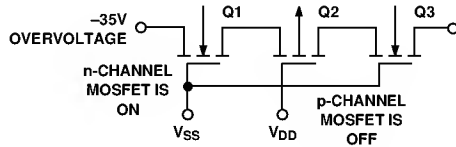


Figure 13. -35 V Overvoltage on an OFF Channel with Multiplexer Power ON

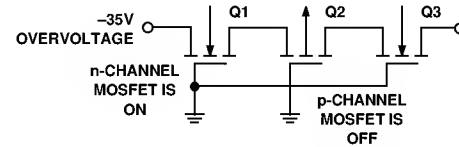
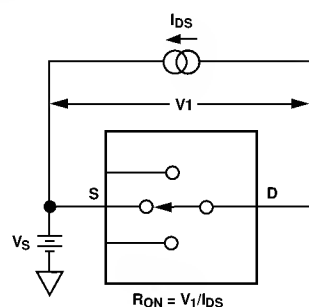


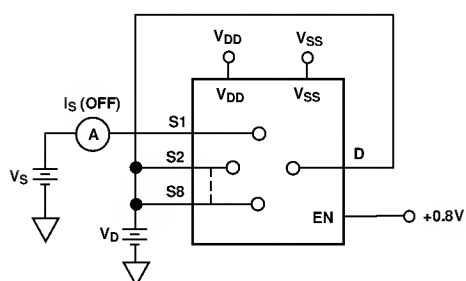
Figure 15. -35 V Overvoltage with Power OFF

ADG508F/ADG509F/ADG528F

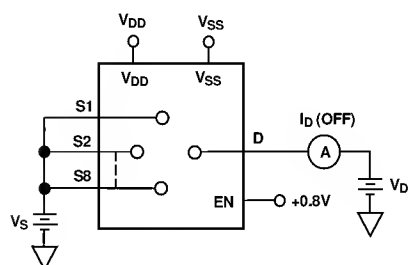
Test Circuits



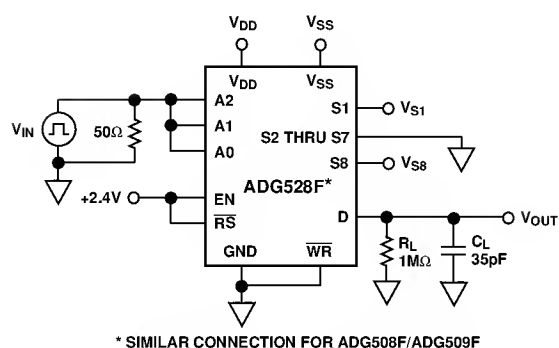
Test Circuit 1. On Resistance



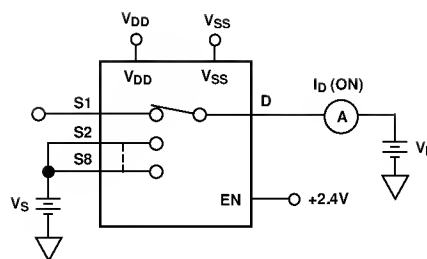
Test Circuit 2. I_S (OFF)



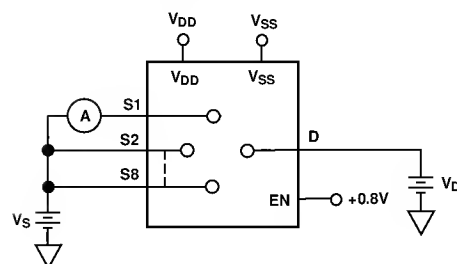
Test Circuit 3. I_D (OFF)



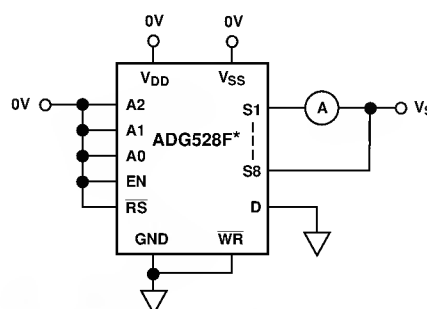
Test Circuit 7. Switching Time of Multiplexer, $t_{TRANSITION}$



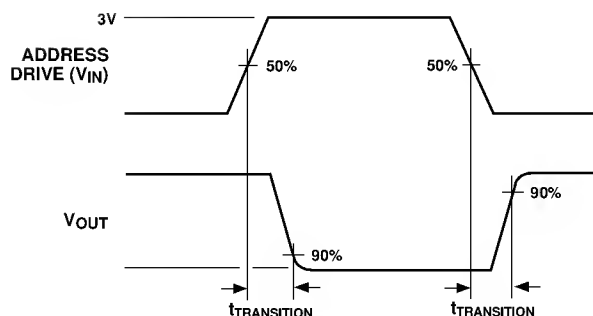
Test Circuit 4. I_D (ON)



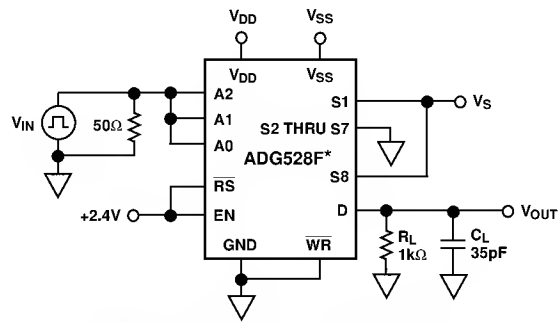
Test Circuit 5. Input Leakage Current (with Overvoltage)



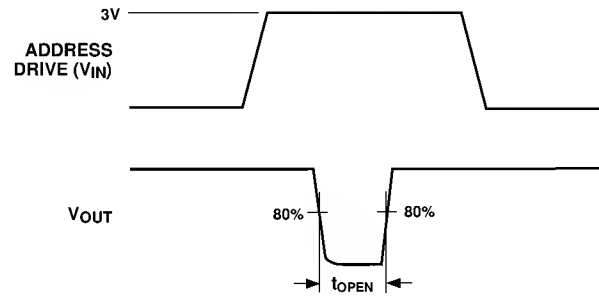
Test Circuit 6. Input Leakage Current (with Power Supplies OFF)



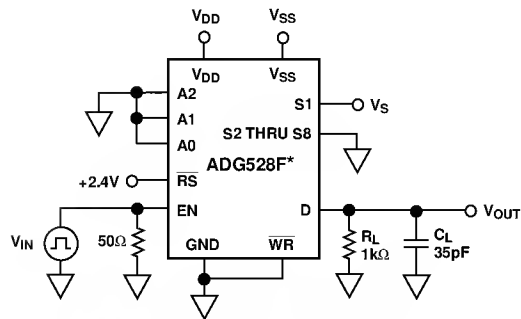
ADG508F/ADG509F/ADG528F



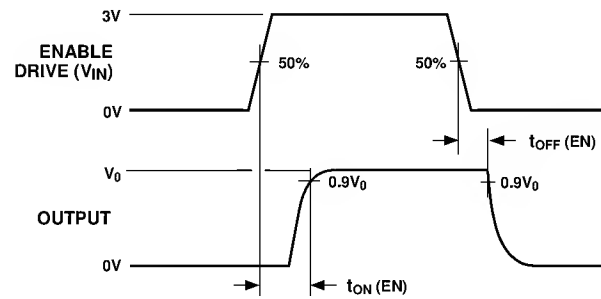
* SIMILAR CONNECTION FOR ADG508F/ADG509F



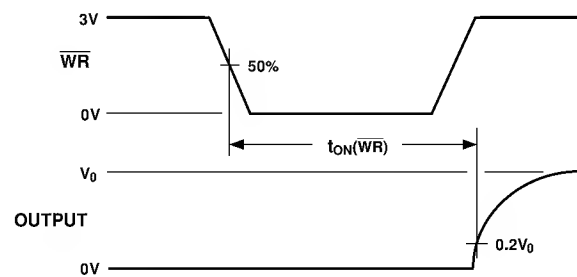
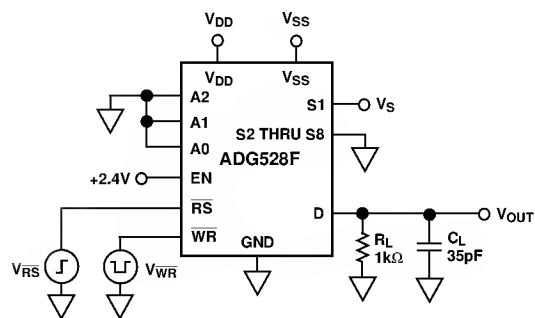
Test Circuit 8. Break-Before-Make Delay, t_{OPEN}



* SIMILAR CONNECTION FOR ADG508F/ADG509F

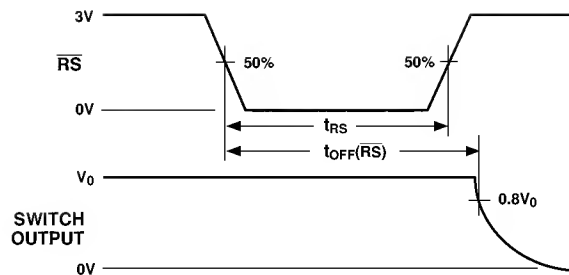
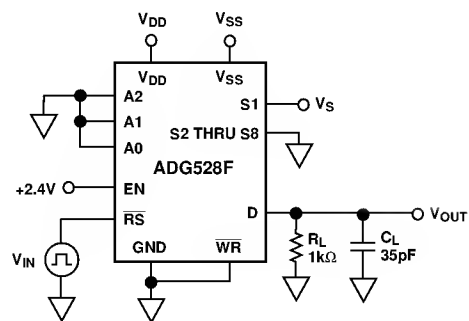


Test Circuit 9. Enable Delay, $t_{ON}(EN)$, $t_{OFF}(EN)$

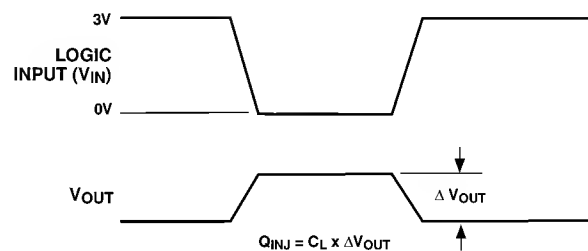
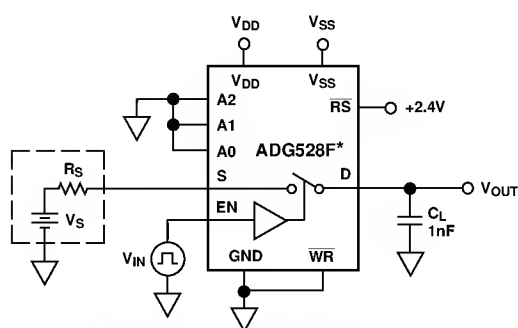


Test Circuit 10. Write Turn-On Time, $t_{ON}(\overline{WR})$

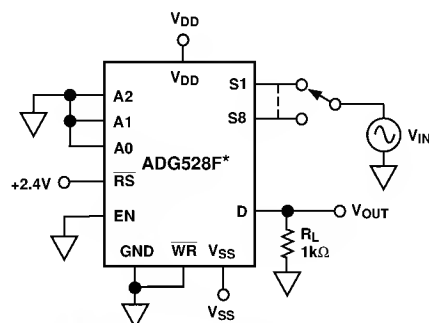
ADG508F/ADG509F/ADG528F



Test Circuit 11. Reset Turn-Off Time, $t_{OFF}(\overline{RS})$



Test Circuit 12. Charge Injection



Test Circuit 13. OFF Isolation

ADG508F/ADG509F/ADG528F

Dimensions shown in inches and (mm).

16-Pin Plastic (N-16)

0.005 (0.13) MIN

0.080 (2.03) MAX

0.310 (7.87)

0.220 (5.59)

16

9

8

PIN 1

0.840 (21.34) MAX

0.060 (1.52)

0.015 (0.38)

0.200 (5.08) MAX

0.200 (5.08)

0.125 (3.18)

0.023 (0.58)

0.014 (0.36)

0.100 (2.54)

0.070 (1.78)

0.030 (0.76)

SEATING PLANE

0.320 (8.13)

0.290 (7.37)

0.015 (0.38)

0.008 (0.20)

15°

0°

BSC

Figure 1: Mechanical drawing of the BSC package. The drawing shows a top view and a side view of the package. The top view includes dimensions for the package body (16x9 mm), pin pitch (0.0500 mm), and pin width (0.0098 mm). The side view shows the package height (0.1574 mm) and the lead height (0.0688 mm). The package is labeled 'PIN 1' and 'BSC'.

The drawing illustrates the mechanical specifications of the 16-pin BSC package. It includes a top view showing the pin layout and package dimensions, a side view showing the package height, and a detail view of the pin profile.

Top View Dimensions:

- Pin 1 indicator
- Pin pitch: 0.118 (0.30)
- Pin width: 0.0500 (1.27)
- Pin thickness: 0.0040 (0.10)
- Package width: 0.4133 (10.50)
- Package length: 0.3977 (10.00)
- Pin 16 position: 0.1618 (4.11)
- Pin 9 position: 0.2992 (7.60)
- Pin 8 position: 0.2914 (7.40)
- Pin 1 position: 0.4193 (10.65)
- Pin 1 position: 0.3937 (10.00)
- Pin 16 position: 0.1043 (2.65)
- Pin 9 position: 0.0926 (2.35)
- Pin 8 position: 0.0291 (0.74)
- Pin 1 position: 0.0098 (0.25) x 45°
- Pin 16 position: 0.0118 (0.30)
- Pin width: 0.0500 (1.27)
- Pin thickness: 0.0040 (0.10)
- Package width: 0.4133 (10.50)
- Package length: 0.3977 (10.00)
- Pin 16 position: 0.1618 (4.11)
- Pin 9 position: 0.2992 (7.60)
- Pin 8 position: 0.2914 (7.40)
- Pin 1 position: 0.4193 (10.65)
- Pin 1 position: 0.3937 (10.00)
- Pin 16 position: 0.1043 (2.65)
- Pin 9 position: 0.0926 (2.35)
- Pin 8 position: 0.0291 (0.74)
- Pin 1 position: 0.0098 (0.25) x 45°

Side View Dimensions:

- Package height: 0.1043 (2.65)
- Pin height: 0.0926 (2.35)
- Pin thickness: 0.0098 (0.25)
- Pin angle: 45°

Detail View Dimensions:

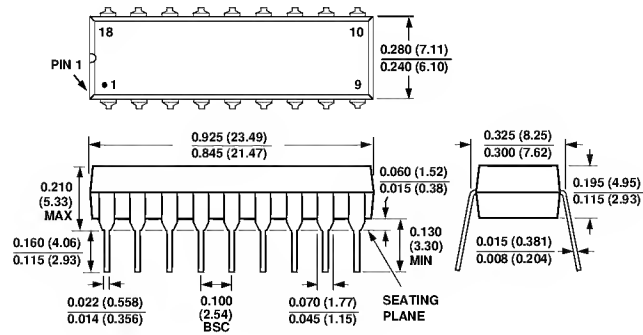
- Pin angle: 8°
- Pin thickness: 0.0125 (0.32)
- Pin angle: 0°
- Pin thickness: 0.0091 (0.23)
- Pin angle: 8°
- Pin thickness: 0.0500 (1.27)
- Pin angle: 0°
- Pin thickness: 0.0157 (0.40)

ADG508F/ADG509F/ADG528F

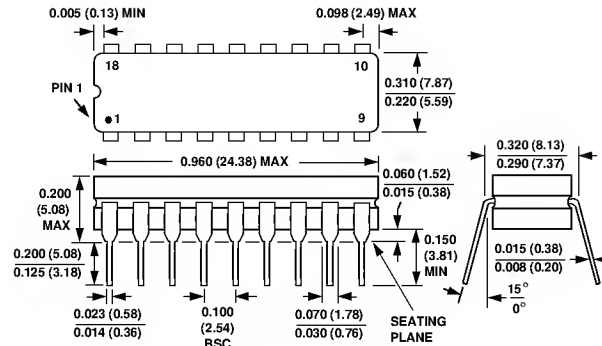
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

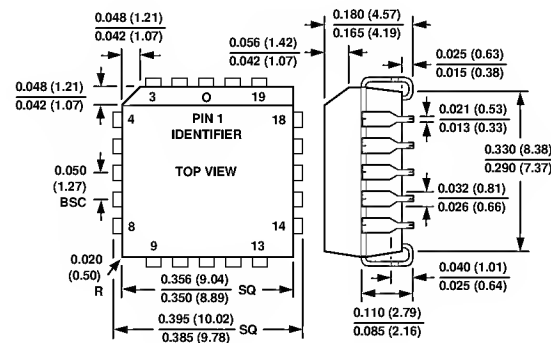
18-Pin Plastic (N-18)



18-Pin Cerdip (Q-18)



20-Pin PLCC (P-20A)



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